Session 3 Overview

TD: Emerging Devices and Circuits

Chair: *Eugenio Cantatore, Philips Research, Eindhoven, The Netherlands*

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The trend to provide increasingly complex electronic applications, to both support and improve one's life, compels the electronics industry to provide more and more processing power in portable and miniaturized, ubiquitous platforms.

The form factor of portable electronics is nowadays determined by the limited energy density offered by batteries. To overcome this limitation, circuit designers need to invent systems with unprecedented power efficiency. The design community is also investigating alternative methods to power circuits, in a continuing effort to improve portability and enable truly pervasive electronics.

On the other hand, novel applications often necessitate the use of novel technologies. Consumer and automotive electronics needs inexpensive and power-efficient interfaces and sensors to communicate effectively with users and monitor the environment, while the quest for smaller, cheaper and higher performance solid-state devices fuels and ensures growth to the electronics industry.

The seven papers in this session offer a broad and exciting perspective on the latest achievements in these fields.

In the first part of the session, devoted to the efficient use of energy, Paper 3.1 from CEA LETI/LITEN presents an important milestone towards truly energy-autonomous microsystems: in the proposed solution, energy scavenged from a thermal source or from electromagnetic radiation is conditioned on-board and used to recharge an above-IC integrated battery. Paper 3.2 from MIT demonstrates a system able to automatically tune the power supply to reach minimum energy operation in a digital circuit. All active components of the control loop, i.e., the energy sensor, the controller and the DC-DC converter used to adapt the supply voltage (featuring >80% efficiency at more than 1μW from a 1.2V primary supply) are integrated in a 65nm technology. Paper 3.3 from U Tokyo and NEC presents an alternative method to achieve energy efficiency, based on the choice of a locally asynchronous, globally synchronous architecture where the power supply is regulated to the minimum value needed to achieve a pre-defined speed performance.

The second part of the session, focusing on novel solid-state devices, begins with two papers presenting the ultimate challenge in terms of device miniaturization: transistors and circuits based on carbon nanotubes. While Paper 3.4 from IBM describes advancements in device and circuit technology enabling complementary carbon nanotube logic and features a functional carbon nanotube ring oscillator. Paper 3.5 from Stanford and USC discusses the performance improvements that circuit designers can expect using carbon nanotubes, instead of ultra-scaled Si CMOS transistors. The session completes with innovative interface devices: Paper 3.6 from MIT and Columbia U discusses a flexible, large-area image sensor based on co-integration of organic semiconductor-based sensors and TFTs and Paper 3.7 from Kyushu U and Bridgestone presents a new, fast e-paper, enabling flexible, bi-stable passive matrix displays, together with its low-power 70V driving circuitry.

3.1 Efficient Power Management Circuit: Thermal Energy Harvesting to Above-IC Microbattery Energy Storage **1:30 PM**

H. Lhermet, CEA LETI, Grenoble, France

An autonomous power generator unit includes 2 micropower sources and their associated management IC; a 1V miniature thermogenerator and RF power receiver are combined with a micropower DC-DC upconverter, power supply manager and microbattery charger, and a 5nW discharge monitor, to manage and store the harvested energy in a 30mm^2 above-IC deposited microbattery.

3.2 Minimum Energy Tracking Loop with Embedded DC-DC Converter Delivering Voltages down to 250mV in 65nm CMOS

Y. Ramadass, Massachusetts Institute of Technology, Cambridge, MA **2:00 PM**

An energy minimization loop, with on-chip energy sensor circuitry, that can dynamically track the minimum energy operating voltage of a digital circuit with changing workload and operating conditions occupies 0.05mm^2 in 65nm CMOS. The DC-DC converter that enables this minimum energy operation can deliver load voltages as low as 250mV and achieved an efficiency >80% while delivering load powers of the order of 1µW and higher from a 1.2V supply.

3.3 LAGS System Using Data/Instruction Grain Power Control **2:30 PM**

M. Ikeda, University of Tokyo, Tokyo, Japan

A locally asynchronous, globally synchronous (LAGS) system with data/instruction grain control is presented for the optimization of power supply voltage, speed performance, PVT and noise tolerance. A LAGS CPU with on-chip DC-DC converter that occupies 250×60µm^2 in 90nm CMOS has 0.98V to 0.68V V_{DD} control with 50ns/85ns transition time and a speedtracing accuracy of 5%.

3.4 Gate Work Function Engineering for Nanotube-Based Circuits **3:15 PM**

Z. Chen, IBM T.J. Watson, Yorktown Heights, NY

The impact of different work function metal gates on the performance of individual nanotube transistors and ultimately an entire nano-circuit is presented. The use of an Al-gate, in the case of a carbon nanotube device, translates directly into a threshold-voltage shift relative to a Pd-gated FET, corresponding to the work function difference between the two metal gates. In this way, a CMOS-type 5-stage ring oscillator on an individual carbon nanotube, is realized without the use of dopants.

3.5 Carbon Nanotube Transistor Circuits: Circuit-Level Performance Benchmarking and Design Options for Living with Imperfections **3:45 PM**

H.-S. Wong, Stanford University, Stanford, CA

One-dimensional carbon nanotube FET (CNFET)-based circuits offer 4.6× faster FO4 speed and 12× energy-delay product improvement over 32nm node Si CMOS (including diameter and doping variations), provided circuits can be built that are immune to misaligned and metallic nanotubes. A design technique that guarantees correct logic operation in the presence of misaligned nanotubes is also presented.

3.6 An Organic Imager for Flexible Large Area Electronics **4:15 PM**

I. Nausieda, Massachusetts Institute of Technology, Cambridge, MA

An active-matrix organic imager suitable for large area flexible electronics is presented. The imager is fabricated using low-temperature (<95°C) processing, producing integrated organic transistors, organic photodetectors, and metal interconnects. Each pixel has a responsivity of 6×10^{-5}A/W and an on/off ratio of 880. The 4×4 array occupies 10.2mm^2 and is powered by a 25V supply.

3.7 Passive-Matrix Flexible Electronic Paper Using Quick-Response Liquid Powder Display (QR-LPD) Technology and Custom Driver Circuits **4:45 PM**

R. Hattori, Kyushu University, Fukuoka, Japan

A low-power high-voltage physically-flexible driver is fabricated for passive-matrix plastic-substrate quick-response liquid powder displays (QR-LPD). A level-shifter circuit effectively reduces the power consumption and the chip area. The 2.3×21.4mm^2 IC is thinned down to 35µm to obtain physical flexibility.